

NM500 preliminary

The NM500 is a **neuromorphic chip** opening new frontiers for smart sensors, IOT, machine learning and cognitive computing. Its neurons can learn and recognize patterns extracted from any data sources such as images, audio waveform, bio signals, text and more, with orders of magnitude less energy and complexity than modern microprocessors.



The NeuroMem[®] neurons are especially suitable to cope with ill-defined and fuzzy data, high variability of context and even novelty detection. Last, but not least, the NM500 is a Wafer Level Chip Scale Package (WLCSP) which can be easily assembled into a network from thousands to millions of neurons, or integrated into an application-specific multi-chip module or 3D stack.

BRAIN-INSPIRED BEHAVIOR

- Recognition and learning latencies are deterministic, in the order of micro-seconds per pattern and independent of the number of neurons in use.
- Neurons are trained by example and decide autonomously when it is necessary to commit a new neuron and/or to correct existing neurons firing erroneously.
- The neurons can behave as a Radial Basis Function (RBF) or a K-Nearest Neighbor (KNN) classifier.
- Winner-takes-all
- Novelty and/or uncertainty can trigger learning. Confusion can be corrected.
- The knowledge built autonomously by the neurons can be saved and restored

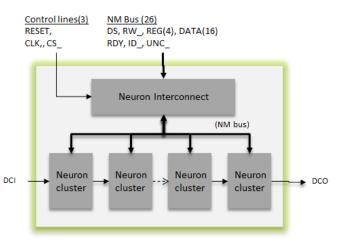
BRAIN-INSPIRED ARCHITECTURE

- A chain of identical elements, operating together with no need for a controller or supervisor.
- Truly parallel architecture interconnecting the neurons intra-chip and inter-chips
- Operates at low clock frequency (37 MHz) and dissipates less than 0.16 Watts
- Multiple chips can be easily assembled to build large networks or expand them later.



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Tel: (02) 2314-2018, 2381-7255 Mobile: 0928-812-548 The NM500 chip is a chain of 576 identical neurons operating in parallel, but also interconnected together to make global decisions. A neuron is a memory with some associated logic to compare an incoming pattern with the reference pattern stored in its memory and react (i.e. fire) according to its similarity range. A neuron also has a couple of attribute registers such as a context and category value. Once a pattern is broadcasted, the neurons communicate briefly with one another (for 16 clock cycles) to determine which one holds the closest match in its memory. The "Winner-Takes-All" neuron de-activates itself when its category is read, thus leaving the lead to the next "Winner-takes-All", if applicable, and so on. A single NM500 delivers the equivalent of 53 GiGaOps per



second when matching a pattern of 256 bytes against 576 models.

Learning is initiated by simply broadcasting a category after an input pattern. If it represents novelty, the next neuron available in the chain automatically stores the pattern and its category. If some firing neurons recognize the pattern but with a category other than the category to learn, they auto-correct their influence fields. This intrinsic inhibitory and excitatory behavior makes the NM500 chip a unique component for cognitive computing applications.

| Recognition speed | Single NM500 @37Mhz | | Chain of NM500 @20Mhz | |
|---|---------------------|------------|-----------------------|------------|
| vector of 256 bytes | μsec | Vector/sec | μsec | Vector/sec |
| Broadcast and Read status | 7.00 | 142,850 | 12.95 | 77,220 |
| Broadcast and Read Best match | 8.00 | 125,000 | 14.80 | 67,568 |
| Broadcast and Read 5 nearest neighbors | 9.95 | 79,300 | 18.40 | 54,348 |
| Broadcast and Read 20 nearest neighbors | 18.86 | 53,009 | 34.90 | 28,653 |

| ANN Attributes | NM500 |
|--------------------|----------------------------------|
| Neuron capacity | 576 |
| Neuron memory size | 256 bytes |
| Categories | 15 bits |
| Distances | 16 bits |
| Contexts | 7 bits |
| Recognition status | Identified, Uncertain or Unknown |
| Classifiers | Radial Basis Function (RBF) |
| | K-Nearest Neighbor (KNN) |
| Distance Norms | L1 (Manhattan), Lsup |

| Electrical and IOs | NM500 |
|--------------------|------------------------------------|
| Clock frequency | 37 MHz for single chip |
| | 18 Mhz for chain of multiple chips |
| I/O | Parallel bus (26 lines) |
| Electrical | 3.3 V I/O operation, 1.2 V core |
| Power consumption | <153 mW in active mode (CS_ low) |
| | at 1.2V and 3.3V |
| Package | 64-pin CSP 4.5x4.5x 0.5 mm |
| | package |

