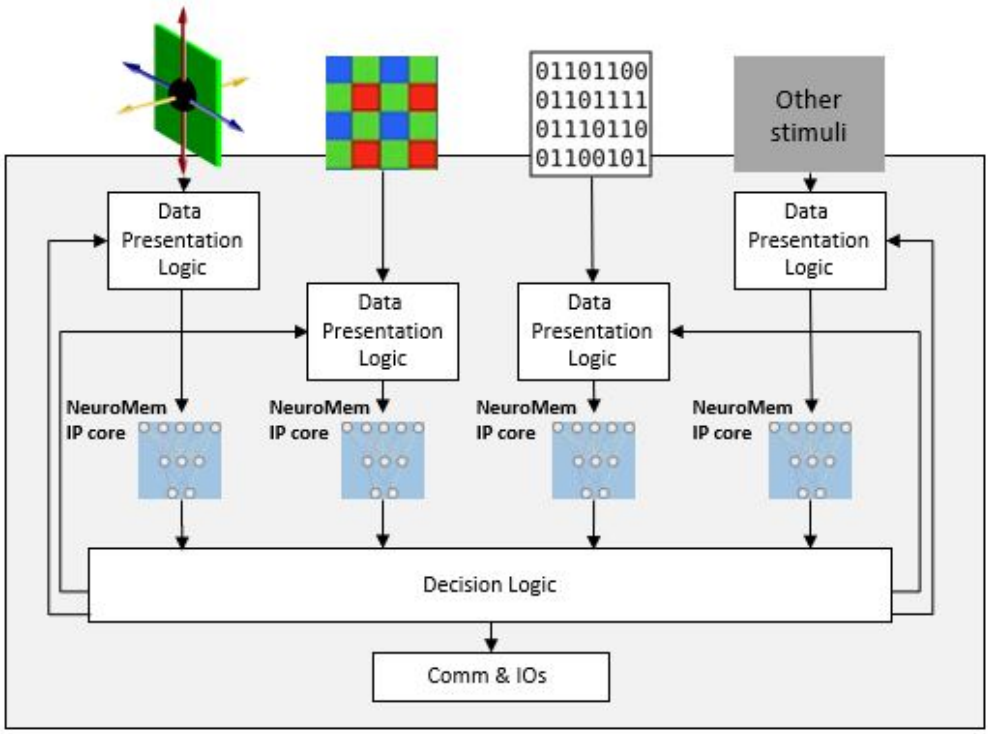
NEUROMEM IP
TO SURF THE 3RD WAVE OF AI

A NeuroMem chip is a bank of identical neuromorphic memory cells (neurons) which react to digital stimuli and can learn and recognize in real-time. They are addressed in parallel and have their own "genetic" material to learn and recall patterns without running a single line of code and without reporting to any supervising unit. This is made possible through a patented parallel bus which allows the neurons to fully collaborate with each other and is the key to accuracy, trainability, and speed performance.

The stimuli, or patterns, broadcasted to the neurons can derive from any data types such as text, scientific datasets, bio-signals, audio files, images and videos, etc.

The applications which can benefit from the NeuroMem chips can be numerous:

- **Number analytics**: stock trading, financials, meteorology, physics, etc.
- **Text analytics**: sentiments analytics, marketing, economics, bioinformatics, etc.
- **Signal analytics**: industrial components, wearables, toys, sports appliances, etc.
- **Video analytics**: face, gesture, surveillance, automotive, building automation, etc.
- **Network security**: secure uplink/downlink, denial of service attack, etc.



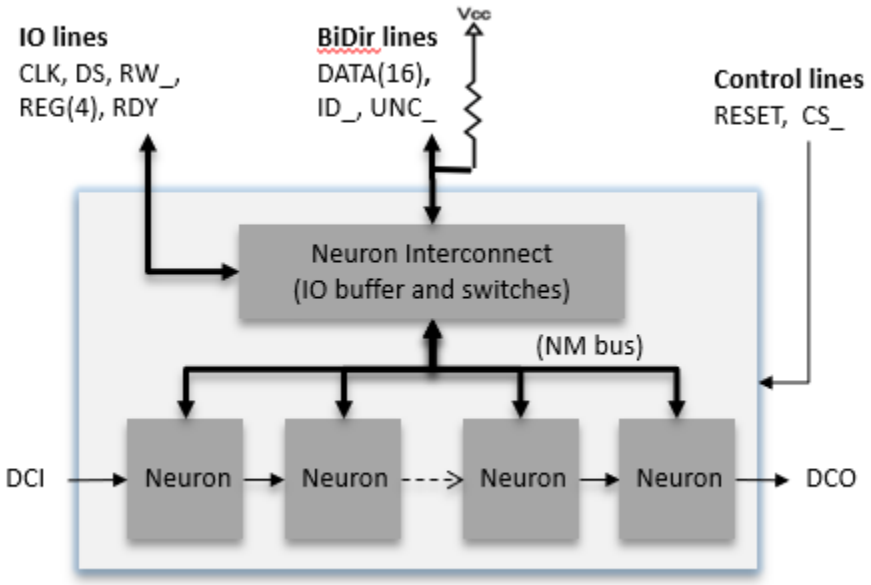
The NeuroMem IP has already been taped-out at 3 different silicon geometry from 130 nm to 28 nm.

ARCHITECTURE

The NeuroMem IP is a fully static CMOS design and composed of two IP cores:

- A Neuron IP core composed of a memory (SRAM), 3000 logic gates and 26 IO lines
- A Neuron Interconnect IP core composed of switches and 26 IO lines

A NeuroMem neural network is an assembly of 1 Neuron Interconnect and N Neuron cores. The Neuron Interconnect connects all the Neurons together, enabling a broadcast mode to all the neurons in parallel, and their necessary interaction for the time of a learning or recognition. The Neurons are also daisy-chained so the next in-line with empty content becomes autonomously the ready-to-learn neuron.



The behavior and architecture of the NeuroMem IP is highly **inspired by the human brain**:

- Queries or stimuli are broadcasted to all the neurons at once
- Neurons autonomously recognize exact or fuzzy matches between the stimuli and their own memory content
- The winner-takes-all and inhibits weaker responders. Responses are auto-sorted per level of confidence
- Two types of classifiers can be selected: K-Nearest Neighbor classifier or Radial Basis Function.
- The neurons know when they do not know and can therefore learn
- The neurons auto-correct themselves if a teacher contradicts their original response
- The neurons operate at low frequency (Mhz) and are energy efficient
- The number of neurons is highly scalable with no impact on the number of I/Os (Inputs/Outputs)
- Finally, the neurons offer a feature which nature cannot reproduce yet and that is the ability to save and restore their knowledge.

NEURON IP CORE

The Neuron IP core is a neuromorphic cell or single neuron. It can be copied as many times as allowed by the floor plan of your FPGA or ASIC. A network of N neurons is designed by daisy-chaining N Neuron IP cores and connecting their 26 IO lines or NeuroMem bus to the Neuron Interconnect module.

Specifications:

- Clock (16-50 Mhz)
- Memory: 256 x 8-bits (default)
- Control logic: 3000 ASIC gates or 4800 FPGA LUTs
    - including 6 registers: Context (8 bits), Category (16 bits), Distance (16 bits), Min and Active Influence Fields (16 bits), Identifier (24 bits).

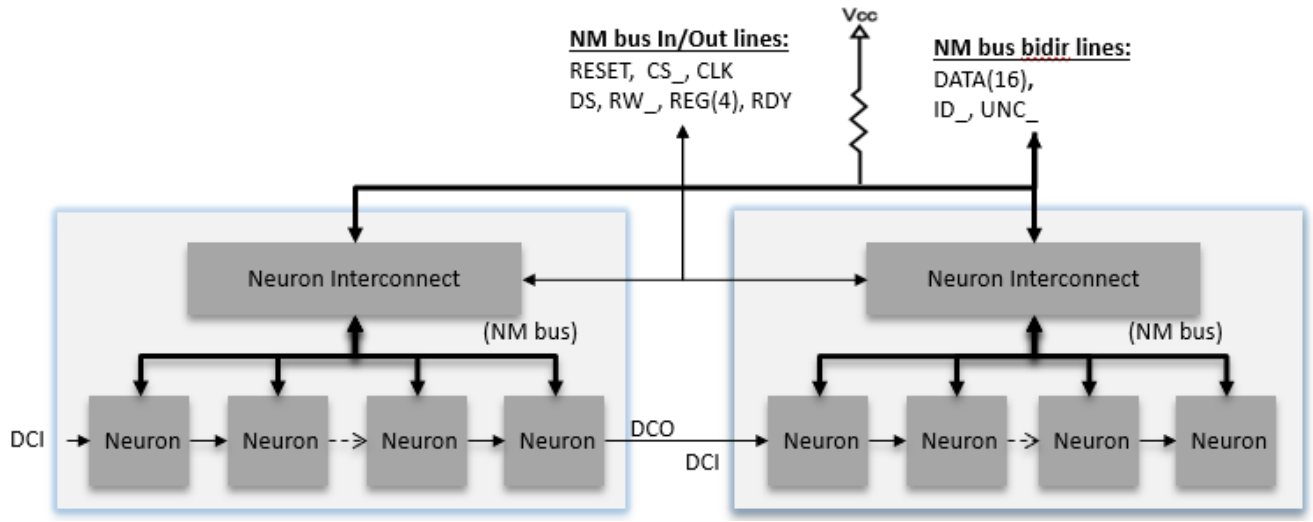
NEURON INTERCONNECT IP CORE

The Neuron Interconnect module is composed of IO buffers and switches. It broadcasts commands to all the neurons at once and interconnects them during learning and recognition. An entire network is controlled by a set of 15 Read/Write commands, including to learn and classify stimuli, save and restore its content.

IO lines or "NeuroMem bus"

CLK	Clock	In
DS	Data strobe line	In
RW_	Read/Write line (default is Read with RW_=1)	In
REG	4 bit register address	In
DATA	16-bit register data (bi-directional)	InOut
RDY	Ready line mixing the ready output signal of all the neurons	Out
ID_	Control line indicating a positive Identified classification	InOut
UNC_	Control line indicating a positive yet Uncertain classification	InOut

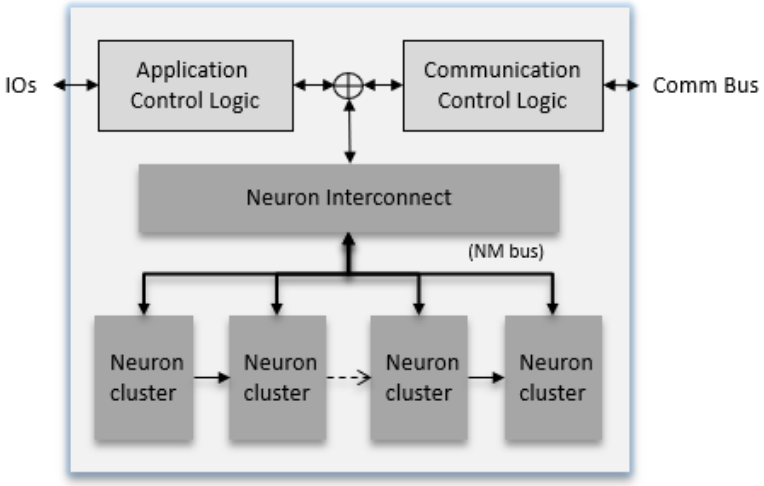
Remark: The NeuroMem bus is the same to interconnect neurons internally and externally as shown in the diagram below:



EXPANDABLE FEATURE SET

Additional IP cores can be added to the NeuroMem IP, such as communication controllers or application specific controllers.

These modules become master of the NeuroMem bus for the time necessary to send stimuli to the neurons and read their responses. Typically, they receive external I/O signals through a custom bus, sample them, extract feature vectors and broadcast them to the neurons for learning and recognition. They can format the responses of the firing neurons for transmission to external actuators or MCU and, if applicable, iterate the process or launch a different process. These modules can handle dual clocks, sampling and manipulating I/O lines at a frequency different than the NeuroMem bus clock.



Example 1: Video recognition MODULE stage

- Direct interface to a digital video signal (8-bit data, Video clock, Line valid, Frame valid)
- Subsampling of a region of interest in the video flow
- Broadcast to the neurons and readout of the classification of the K closest neurons
- On/Off switch of the recognition stage for power saving

Example 2: Signal recognition MODULE stage

- Direct interface to a digital signal received over SPI or I2C
- Sampling of the signal in real time
- Broadcast to the neurons and readout of the classification of the K closest neurons
- On/Off switch of the recognition stage for power saving

Example 3: PCIe controller

- High speed data throughput
- Vector cruncher for batch learning and recognition

LICENSE MODELS

Licenses can be granted on a single project or multiple projects basis. Payment includes an upfront licensing fee, a % royalty of the invoiced selling price of the final products, and a yearly maintenance subscription.

The typical scope of a license is a product including the Licensed IP in combination with other IP blocks available from the Licensee or other party; whether offered as (i) System-on-Chip (SOC); (ii) Multi-Chip Package (MCP), Multi-Chip Module (MCM) and FPGA

FPGA IP

- Netlist of the Licensed modules (EDIF or vendor equivalent file format) installed on a compatible FPGA board (Xilinx, Altera, Lattice)
- Modules' connection in readable Verilog allowing multiple instantiations and different routing on the SOC
- Full test benches (Verilog) for both verification and production
- 10 hours free support via phone and e-mail to be used within 12 months

GDSII IP

- GDSII file of the licensed modules, after customization and adaptation to the Product Development Kit (PDK) of the selected foundry
- Full test benches (Verilog) for both verification and production
- Technical assistance for 30 days

Encrypted IP

- Encrypted Verilog code for the licensed modules, foundry library independent
- Modules' connection in readable Verilog allowing multiple instantiation on the SOC
- Full test benches (Verilog) for both verification and production
- Technical assistance for 60 days for adaptation to specific foundry library

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康普企業有限公司

台北市和平西路二段141 號6 樓之4
Email: CECL@seed.net.tw
http://www.compton.com.tw

Tel: (02) 2314-2018, 2381-7255
Mobile: 0928-812-548